CLAIMS

23. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of said plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions;

generating, in response to said one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal inactive state corresponding to

said one or more second selected assertion and de-assertion states of said one or more clock control signals.

24. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

25. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

26. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

27. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a

deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

28. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

29. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

30. *(PREVIOUSLY PRESENTED)* The method of claim 23, wherein said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

31. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising:

generating said one or more local control signals having another one or

more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions; and

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock control signals having another one or more respective assertion and de-assertion states.

32. *(PREVIOUSLY PRESENTED)* The method of claim 23, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

33. *(PREVIOUSLY PRESENTED)* The method of claim 23, further comprising generating a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

34. *(PREVIOUSLY PRESENTED)* The method of claim 23, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

35. *(PREVIOUSLY PRESENTED)* The method of claim 23, wherein

said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local control signals.

36. *(PREVIOUSLY PRESENTED)* The method of claim 23, wherein said generating, in response to said one or more clock control signals, at least said first clock signal further comprises generating a second clock signal having active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

37. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of said plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions;

generating, in response to said one or more local control signals, one or

more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

38. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

39. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

40. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data

states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

41. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

42. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

43. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

44. *(PREVIOUSLY PRESENTED)* The method of claim 37, wherein

said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

45. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising:

generating said one or more local control signals having another one or more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions;

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock control signals having another one or more respective assertion and de-assertion states; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

46. *(PREVIOUSLY PRESENTED)* The method of claim 37, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

47. *(PREVIOUSLY PRESENTED)* The method of claim 37, further comprising generating a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

48. *(PREVIOUSLY PRESENTED)* The method of claim 37, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

49. *(PREVIOUSLY PRESENTED)* The method of claim 37, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local control signals.

50. *(PREVIOUSLY PRESENTED)* The method of claim 37, wherein said generating, in response to said one or more clock control signals, at least said first clock signal further comprises generating a second clock signal having active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

51. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles, on one or more of said plurality of incoming instructions for data

processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of said plurality of first clock signal cycles, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to at least a second one subsequent to said first one of said plurality of first clock signal cycles, said one or more decoded instructions;

generating, in response to said one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals.

52. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of

data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

53. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

54. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

55. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

56. *(PREVIOUSLY PRESENTED)* The method of claim 51, further

comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

57. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

58. *(PREVIOUSLY PRESENTED)* The method of claim 51, wherein said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

59. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising:

generating said one or more local control signals having another one or more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another

one or more respective portions of said one or more of said plurality of incoming instructions; and

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock control signals having another one or more respective assertion and de-assertion states.

60. *(PREVIOUSLY PRESENTED)* The method of claim 51, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

61. *(PREVIOUSLY PRESENTED)* The method of claim 51, further comprising generating a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

62. *(PREVIOUSLY PRESENTED)* The method of claim 51, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

63. *(PREVIOUSLY PRESENTED)* The method of claim 51, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local control signals.

64. *(PREVIOUSLY PRESENTED)* The method of claim 51, wherein said generating, in response to said one or more clock control signals, at least said

first clock signal further comprises generating a second clock signal having active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

65. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having an active state with a plurality of successive cycles and an inactive state with substantially zero cycles, on one or more of said plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to at least a first one of said plurality of first clock signal cycles, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to at least a second one subsequent to said first one of said plurality of first clock signal cycles, said one or more decoded instructions;

generating, in response to said one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion

states of said one or more local control signals; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction.

66. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

67. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

68. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

69. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

70. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

71. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

72. *(PREVIOUSLY PRESENTED)* The method of claim 65, wherein said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

73. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising:

generating said one or more local control signals having another one or more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions;

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock control signals having another one or more respective assertion and de-assertion states; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

74. *(PREVIOUSLY PRESENTED)* The method of claim 65, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

75. *(PREVIOUSLY PRESENTED)* The method of claim 65, further comprising generating a status signal indicative of said one or more respective

assertion and de-assertion states of said one or more local control signals.

76. *(PREVIOUSLY PRESENTED)* The method of claim 65, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

77. *(PREVIOUSLY PRESENTED)* The method of claim 65, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local control signals.

78. *(PREVIOUSLY PRESENTED)* The method of claim 65, wherein said generating, in response to said one or more clock control signals, at least said first clock signal further comprises generating a second clock signal having active and inactive states substantially independent of said one or more respective assertion and de-assertion states of said one or more clock control signals.

79. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of said plurality of incoming instructions for data processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding

to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions;

generating, in response to said first clock signal, a second clock signal and said one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals with said second selected assertion and de-assertion states following reception of said power management instruction; and

generating, in response to said one or more clock control signals, said first and second clock signals with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.

80. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

81. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

82. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

83. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

84. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in

response to said one or more local control signals, one or more clock control signals.

85. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

86. *(PREVIOUSLY PRESENTED)* The method of claim 79, wherein said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

87. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising:

generating said one or more local control signals having another one or more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another one or more respective portions of said one or more of said plurality of incoming instructions; and

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock

control signals having another one or more respective assertion and de-assertion states.

88. *(PREVIOUSLY PRESENTED)* The method of claim 79, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

89. *(PREVIOUSLY PRESENTED)* The method of claim 79, further comprising generating a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

90. *(PREVIOUSLY PRESENTED)* The method of claim 79, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

91. *(PREVIOUSLY PRESENTED)* The method of claim 79, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local control signals.

92. *(PREVIOUSLY PRESENTED)* A method for processing electronic data, comprising:

receiving at least a plurality of incoming instructions, including a power management instruction, from at least one signal source;

selectively operating, in response to a first clock signal having active and inactive states, on one or more of said plurality of incoming instructions for data

processing by

generating one or more decoded instructions and one or more local control signals having one or more respective assertion and de-assertion states including one or more first selected assertion and de-assertion states corresponding to said power management instruction by performing, with a first portion of pipeline subcircuitry included in a plurality of subcircuits in response to said active first clock signal, at least one or more respective portions of one or more processing, including decoding, operations upon at least one or more respective portions of said one or more of said plurality of incoming instructions, and

executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions;

generating, in response to said first clock signal, a second clock signal and said one or more local control signals, one or more clock control signals having one or more respective assertion and de-assertion states including one or more second selected assertion and de-assertion states corresponding to said one or more first selected assertion and de-assertion states of said one or more local control signals; and

generating, in response to said one or more clock control signals, said first and second clock signals with said first clock signal inactive state corresponding to said one or more second selected assertion and de-assertion states of said one or more clock control signals and following reception of said power management instruction, and with said second clock signal having active and inactive states substantially independent of said one or more second selected assertion and de-assertion states of said one or more clock control signals.

93. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of

data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

94. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising retaining, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

95. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

96. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising retaining, until a reactivation of said first clock signal, with data storage circuitry included in said plurality of subcircuits in response to a deactivation of said first clock signal, a plurality of data having respective data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

97. *(PREVIOUSLY PRESENTED)* The method of claim 92, further

comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more local control signals, one or more clock control signals.

98. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising generating, with data storage circuitry included in said plurality of subcircuits in response to a reactivation following a deactivation of said first clock signal, a plurality of data having respective retained data states determined by said execution of said one or more decoded instructions prior to said generating, in response to said one or more clock control signals, at least said first clock signal.

99. *(PREVIOUSLY PRESENTED)* The method of claim 92, wherein said generating one or more decoded instructions and one or more local control signals comprises performing said at least one or more respective portions of one or more processing, including decoding, operations with decoding circuitry.

100. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising:

generating said one or more local control signals having another one or more respective assertion and de-assertion states including one or more third selected assertion and de-assertion states corresponding to one of said one or more of said plurality of incoming instructions other than said power management instruction by performing, with said first pipeline subcircuitry portion in response to said active first clock signal, at least another one or more respective portions of said one or more processing, including decoding, operations upon at least another

one or more respective portions of said one or more of said plurality of incoming instructions;

generating, in response to said one or more third selected assertion and de-assertion states of said one or more local control signals, said one or more clock control signals having another one or more respective assertion and de-assertion states; and

generating, in response to said one or more clock control signals, at least said first clock signal with said first clock signal active state corresponding to said another one or more respective assertion and de-assertion states of said one or more clock control signals.

101. *(PREVIOUSLY PRESENTED)* The method of claim 92, wherein said executing, with a second portion of said pipeline subcircuitry in response to said active first clock signal, said one or more decoded instructions comprises executing said one or more decoded instructions with arithmetic logic circuitry.

102. *(PREVIOUSLY PRESENTED)* The method of claim 92, further comprising generating a status signal indicative of said one or more respective assertion and de-assertion states of said one or more local control signals.

103. *(PREVIOUSLY PRESENTED)* The method of claim 92, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises logically converting said one or more local control signals to said one or more clock control signals.

104. *(PREVIOUSLY PRESENTED)* The method of claim 92, wherein said generating, in response to said one or more local control signals, one or more clock control signals comprises storing and reading out said one or more local

control signals.